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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,512	06/15/2001	Michael Keaveney	T0461/7015 SJH	8326

23628 7590 12/17/2004

WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,512	KEAVENEY ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,20-24,26 and 27* is/are rejected.

7)☒ Claim(s) *18,19 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are pending in the instant application.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. *The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided.* The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Objections

4. Claims 1-29 are objected to because of the following informalities:

Regarding claim 1, in line 12, "input to clock input" should be replaced by "input to the clock input", in line 13, "input to clock input" should be replaced by "input to the clock input", and, in line 14, "input to the second storage" should be replaced by –input of the second storage--. Further, "the delay" in line 14 is lacking proper antecedent basis. It is suggested that "the delay" in line 14 is replaced by "the delay element".

Regarding claim 7, in line 2, "coupled by a" should be replaced by –coupled to a-.

Regarding claim 9, in line 1, "relative delay in the trailing edges" should be replaced by –relative delay between the trailing edges--.

Regarding claim 11, in line 13, "first input to the charge pump" should be replaced by –first input of the charge pump", in line 15, "second input to the charge pump" should be replaced by –second input of the charge pump--, in line 23, "input to clock" should be replaced by –input to the clock--, in line 24, "input to clock" should be replaced by –input to the clock--, and in line 27, "the two outputs" should be replaced by –the two outputs of the storage elements—to clarify the claim language.

Regarding claim 13, in line 5, "storage element" should be replaced by –storage elements--, and, in line 16, "the trailing edge" should be replaced by –a trailing edge— because it lacks antecedent basis.

Regarding claim 25, the claim is objected to because the additional stretching element is not limited to a particular connection in the apparatus. To make the claim clearly definite, the additional stretching element should be coupled appropriately into the apparatus such that one having ordinary skill in the art could make a definite interpretation as to the placement of the element.

Regarding claim 27, in line 4, "controllable oscillator device" should be replaced by –a controllable oscillator device--.

Regarding claim 29, the claim is objected to because, with exception of the first and second inputs of the charge pump being respectively coupled to the outputs of the first and second storage elements, the remaining limitations of the claim are not further limiting. The claim limitations which do not further limit parent claim 27 should be removed from the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 10 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 10, the claim is indefinite for failing to apply a reference for the amount of maximum deviation. The claim relates to having a relative delay greater than the maximum deviation of the phase of the second storage element's clock input. However, to be definite, the maximum deviation of the phase must be made with respect to something known. Further, the concepts of a phase deviation and a delay of time are not strictly analogous, and the claim language thereby makes the claim indefinite because it is unclear how an amount of time is to be made greater than an amount of phase difference.

Claim 24 is rejected for the same reasons as applied to claim 10 above.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Shurboff (US 6049233).

Regarding claim 11, Shurboff discloses a phase lock loop (fig. 11) apparatus having a reference signal input (F_R) and an oscillator output (fig. 11, ref. 1112), the apparatus comprising: a) a filter element (fig. 11, ref. 1102) having an input and an output, b) controllable oscillator device or VCO (fig. 11, ref. 1104) having a control input coupled to the output of the filter element and an output adapted to produce the oscillator output, a frequency dividing element (fig. 11, ref. 1106) having a first input coupled to the output of the oscillator output and an output for producing a feedback loop signal (fig. 11, ref. F_V), d) a charge pump (fig. 1, refs. 106 and 108) having two inputs (fig. 1, ref. 140 and 144) and an output (fig. 1, ref. 142) adapted to provide a phase difference signal as an input to the filter element, and e) a phase detection apparatus (fig. 1, refs. 102, 104, and 118) having a first input (fig. 1, ref. 122) for the reference signal, and a second input (fig. 1, ref. 132) for the loop feedback signal, the apparatus comprising: i) a first storage element (fig. 1, ref. 102) having a clock input (fig.1, ref. 122), a reset input (fig. 1, ref. 124) and an output (fig. 1, ref. 126) coupled to

the first input of the charge pump (fig. 1, ref. 140), ii) a second storage element (fig. 1, ref. 104) having a clock input (fig. 1, ref. 132), a reset input (fig. 1, ref. 134) and an output (fig. 1, ref. 136) coupled to the second input of the charge pump (fig. 1, ref. 144), iii) a logic element (fig. 1, ref. 118) for logically combining the outputs of the first and second storage elements, the logic element having inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element, a delay element (fig. 1, ref. 114) coupled to the output of the logic element, the delay element having an output coupled to the reset element of the second storage element, and wherein the reference signal (F_R) is input to the clock input of the first storage element and the loop feedback signal (F_V) is input to the clock input of the second storage element (fig. 1), the provision of the delay at the reset input to the second storage element effecting a delay of a trailing edge of the output of the second storage element relative to a trailing edge of the output of the first storage element, the two outputs being coupled to the inputs to the charge pump. It is inherent that the delay of the reset of the second storage register will cause a delay of a trailing edge of the output of the second storage element. The limitations of the claim are fully embodied by the combination of figures 1 and 11. In figure 11, the phase detector 500 may be embodied by the phase detector and charge or current pump in any one of figures 1, 5 or 10 of Shurboff as understood by one having skill in the art.

9. Claims 13 and 20-24, 26, 27 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Iga et al (US 5459755; hereafter "Iga")

Regarding claim 13, Iga discloses a phase detection apparatus (abstract) by figure 1 comprising: a first storage element (T4-T6) having a clock input (I1), a reset input (output of T1 taken as input to T4) and an output (output of T4), a second storage element (T7-T9) having a clock input (I2), a reset input (output of T2 taken as input to T9) and an output (output of T9), a logic element (T3) for logically combining the outputs of the first and second storage elements, the logic element having two inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element and the reset input of the second storage element (coupled through T1 and T2), and a stretching element (DELAY CIRCUIT 3') for effecting a stretching of the trailing edge of the output of one of the first and second storage elements (col. 4, lines 1-20). The first storage element and second storage elements consist of the NAND gates T4-T6 and T7-T9 respectively. The reset inputs of the first and second storage elements are the feedback signals from NAND gates T1 and T2 into gates T4 and T9 respectively which are controlled by the logic element output S3 of T3. Further, as disclosed by Iga, the delay element (3') is used to create a linear response of the phase detection apparatus by introducing a delay which will cause a pulse stretching of the outputs of the first and second storage elements according to the amount of current supplied by the current source (col. 3, lines 53-58). The pulse stretching occurs because the reset of NAND gates T1 and T2 is delayed. Therefore, when less current is being supplied by the current source, the delay is lengthened and pulse stretching occurs to improve the linearity of the phase detector.

Regarding claim 20, Iga discloses the limitations of claim 13 as applied above. Further, Iga discloses that, as broadly as claimed, the stretching element (fig. 1, ref. 3') is located or coupled to the output of the first storage element (fig. 1, refs. T4-T6).

Regarding claim 21, Iga discloses the limitations of claim 13 as applied above. Further, Iga discloses that, as broadly as claimed, the stretching element (fig. 1, ref. 3') is located or coupled to the output of the second storage element (fig. 1, refs. T7-T9).

Regarding claim 22, Iga discloses the limitations of claim 13 as applied above. Further, as broadly as claimed, the phase detector of Iga is a tri-state phase frequency detector for at least the reasons that the phase detector of the instant application is a tri-state phase frequency detector because the phase detector of the instant application and that of Iga are substantially identical in form and function.

Regarding claim 23, Iga discloses the limitations of claim 13 as applied above. Further, Iga discloses that the delay in the trailing edge is programmable because the delay is programmed or controlled by the amount of current Ic in the current source (col. 5, lines 49-58).

Regarding claim 24, Iga discloses the limitations of claim 23 as applied above. Further, because the purpose of the delay is to remove the non-linear region of operation from the phase detection apparatus, it is obvious that the delay would be at least as long as the time difference between the maximum deviation of the phase difference of the second element's clock input. As understood by one having ordinary skill in the art, at the time of phase lock, the delay must be at least great enough to overcome the region of non-linearity. Therefore, it would have been obvious to one

having ordinary skill in the art at the time which the invention was made to utilize a delay at least as great as the time difference between the maximum deviation in phase of the clock input to the second storage element because it would allow the region of non-linearity to be overcome even during a period of phase lock.

Regarding claim 26, Iga discloses the limitations of claim 13 as applied above. Further, Iga discloses by figure 1 that the phase detection apparatus of claim 13 is used in a phase locked loop (fig. 1; abstract) having a reference or input signal (I1; col. 5, lines 15-20) and a loop feedback signal or reference signal (I2; col. 5, lines 15-20) and wherein the reference signal (I1) is input to the clock input of the first storage element (T4-T6) and the loop feedback signal (I2) is input to the clock input of the second storage element (T7-T9), and the provision of the stretching element for stretching the trailing edge of the output of one of the first and second storage elements enables the introduction of a compensatory phase offset at the input of the phase detection apparatus when the apparatus is used as a phase frequency detector in a phase locked loop (col. 4, lines 1-20). Although Iga discloses in figure 1 that the feedback signal or output of the frequency divider is I1, it is noted by the Examiner that the specification of Iga discloses that I2 is the reference or feedback signal. It is suggested by the Examiner that, in the drawing of Iga, the feedback signal output from the frequency divider labeled I1 should rather be labeled I2 as suggested by the specification (col. 5, lines 15-20). With the feedback signal of the phase lock loop apparatus of Iga appropriately applied to the second storage means as reasonably suggested by the

Examiner to accommodate for the apparent discrepancy in the disclosure of Iga, the limitations of claim 25 are disclosed by Iga.

Regarding claim 27, Iga discloses a phase lock loop apparatus by figure 1 (abstract) having a reference signal input (I1) and an oscillator output (S2), the apparatus comprising: a) a filter element (1) having an input (S31) and an output (V1), b) a controllable oscillator device (2) having an input coupled to the output of the filter element and an output (S2) adapted to produce the oscillator output, c) a frequency dividing element (4) having a first input coupled to the output of the oscillator output and an output for producing a feedback loop signal, d) a charge pump (31; T11 and T12) having two inputs (Q1 and Q2) and an output (S31) adapted to provide a phase difference signal as an input to the filter element, and e) a phase detection apparatus (30') comprising: i) a first storage element (T4-T6) having a clock input coupled to the reference signal input (I1), a reset input (output of T1 taken as input to T4) and an output (output of T4), ii) a second storage element (T7-T9) having a clock input (I2) coupled to the loop feedback signal, a reset input (output of T2 taken as input to T9) and an output (output of T9), iii) a logic element (T3) for logically combining the outputs of the first and second storage element, the logic element having two inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element and the reset input of the second storage element, and iv) a stretching element (3') for effecting a stretching of the trailing edge of the output of one of the first and second storage elements, and wherein the outputs of the first and second storage elements are coupled to the inputs of the charge pump. The first

storage element and second storage elements consist of the NAND gates T4-T6 and T7-T9 respectively. The reset inputs of the first and second storage elements are the feedback signals from NAND gates T1 and T2 into gates T4 and T9 respectively which are controlled by the logic element output S3 of T3. Although Iga discloses in figure 1 that the feedback signal or output of the frequency divider is I1, it is noted by the Examiner that the specification of Iga discloses that I2 is the reference or feedback signal. It is suggested by the Examiner that, in the drawing of Iga, the feedback signal output from the frequency divider labeled I1 should rather be labeled I2 as suggested by the specification (col. 5, lines 15-20). With the feedback signal of the phase lock loop apparatus of Iga appropriately applied to the second storage means as reasonably suggested by the Examiner to accommodate for the apparent discrepancy in the disclosure of Iga, the limitations of claim 27 are disclosed by Iga.

Regarding claim 29, Iga discloses the limitations of claim 27 as applied above. Further, Iga discloses by figure 1 that the outputs of the first and second storage elements (Q1 and Q2) are connected respectively to the first and second inputs of the charge pump (31).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shurboff.

Regarding claim 1, Shurboff discloses by figure 1 a phase detection apparatus (abstract) for generating a phase difference signal for use in a phase lock loop (PLL), the apparatus having a first input (132) for a reference signal, and a second input (122) for a loop feedback signal, the apparatus comprising: a) a first storage element (104) having a clock input (132), a reset input (134) and an output (136), b) a second storage element (102) having a clock input (122), a reset input (124) and an output (126), c) a logic element (118) for logically combining the outputs of the first and second storage elements, the logic element having inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element, d) a delay element (110) coupled to the output of the logic element (118), the delay element having an output coupled to the reset element (124) of the second storage element (102), the provision of the delay element (110) at the reset input of the second storage element effecting a delay of a trailing edge of the output of the second storage element relative to a trailing edge of the output of the first storage element. It is inherent that the delay of the reset of the second storage register will effect a delay of a trailing edge of the output of the second storage element. In the particular disclosure of Shurboff, the reference signal (F_R) is applied to the input clock of the second storage element rather than that of the first storage element as claimed, and likewise, the feedback signal (F_V) is applied to the clock input of the first storage element rather than that of the second storage element as claimed. However, as understood by one having ordinary skill in the

art, the difference between the disclosure of Shurboff and that of the instant invention are such that the difference could reasonably be considered a matter of design choice. The Applicant has not disclosed that the particular input of the reference and feedback signals to storage elements provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the disclosed reference and feedback connections as disclosed by Shurboff because the nature of the phase detector is simply to ascertain any difference between two input phases. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to apply the reference input to the first storage input and the feedback signal to the second storage element because in the case of inputs to a phase detector the order of the inputs is not consequential to the function of the phase detector as reasonably understood by one having ordinary skill in the art and it would be considered a matter of design choice.

Regarding claim 2, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses by figure 1 a second delay element (114) with an input coupled to the output of the logic element (118), the second delay element having an output (152) coupled to the reset element of the first storage element (134) and wherein the delay introduced by the second delay element to the first storage element is less than the delay introduced by the first delay element to the second storage element. Because the delay of the second delay element (114) is the only delay applied to the reset of the first storage device and both the delays of the first and second delay

elements (110 and 114, respectively) are applied to the reset of the second storage element, the delay introduced by the second delay element to the first storage element is less than the delay introduced by the first delay element to the second storage element because the delays are additive.

Regarding claim 3, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses by figure 1 a second delay element (114) coupled between the logic element (118) and the first delay element (110), the output of the second delay element being coupled to the reset element of the first storage element and the input of the first delay element.

Regarding claim 4, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses that the logic element comprises a logic AND gate (fig. 1, ref. 118; col. 2, lines 12-20)).

Regarding claim 5, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses that the two storage elements (fig. 1, refs. 102 and 104) are flip flops (col. 2, lines 12-20).

Regarding claim 6, Shurboff discloses the limitations of claim 5 as applied above. Shurboff further discloses that the flip flops are D type flip flops and that the inputs of the flip flops are coupled to logic high (col. 2, lines 12-30).

Regarding claim 7, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses by figure 1 that the output of the first storage element (136) and the output of the second storage element (126) are coupled to a first current source (108) (col. 2, lines 30-45) having an enable input (144) coupled to the output of the first

storage element and a second current source (106) having an enable input (140) coupled to the output of the second storage element, the first and second current sources being coupled to form an output (142, "CURRENT OUTPUT) for a phase difference signal.

Regarding claim 8, Shurboff discloses the limitations of claim 1 as applied above. Further, as broadly as claimed, the phase detector of Shurboff is a tri-state phase frequency detector for at least the reasons that the phase detector of the instant application is a tri-state phase frequency detector because the phase detector of the instant application and that of Shurboff are substantially identical in form and function.

12. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shurboff in view of Gailbreath, Jr. (US 4795985; hereafter "Gailbreath").

Regarding claim 9, Shurboff discloses the limitations of claim 1 as applied above. Although Shurboff discloses that the delay element creates a relative delay, Shurboff does not explicitly disclose that the relative delay is programmable. However, Gailbreath teaches a phase locked loop using a programmable delay line (fig. 1, ref. 12; abstract). Gailbreath teaches that the programmable delay line provides up to 66ns of delay in 2ns steps. Gailbreath further teaches that the programmable delay may be programmed to delay in the direction that minimizes the phase error between the data transitions and reference clock. (col. 1. line 60 – col. 2, line 8). In the case of the invention of Shurboff, the delay lines could be of the programmable type to appropriately accommodate for minimizing phase differences and properly adjusting the linearity of the output characteristic of the charge pump. One skilled in the art would

properly understand the advantages of a programmable delay line being that the system could be more appropriately and efficiently tailored. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize programmable delay lines as taught by Gailbreath as the delay elements of Shurboff because the delay lines could be easily tailored to minimize phase differences and assist in creating a linear output characteristic of the charge pump.

Regarding claim 10, Shurboff in view of Gailbreath disclose the limitations of claim 9 as applied above. Further, because the purpose of the delay is to remove the non-linear region of operation from the phase detection apparatus, it is obvious that the delay would be at least as long as the time difference between the maximum deviation of the phase difference of the second element's clock input. As understood by one having ordinary skill in the art, at the time of phase lock, the delay must be at least great enough to overcome the region of non-linearity. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a delay at least as great as the time difference between the maximum deviation in phase of the clock input to the second storage element because it would allow the region of non-linearity to be overcome even during a period of phase lock.

13. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shurboff in view of Eriksson (US 5986512).

Regarding claim 12, Shurboff discloses the limitations of claim 11 as applied above. Shurboff discloses the frequency dividing element, but does not explicitly disclose that the frequency dividing element comprises an interpolator. However,

Eriksson teaches an analogous phase lock loop apparatus wherein the frequency divider is an interpolator or fractional-N modulator (fig. 1, refs. 28 and 38; col. 2, lines 47-63). Eriksson teaches that the use of an interpolator is advantageous because it can create a PLL having a higher frequency resolution and a higher bandwidth. Further, Eriksson teaches that the interpolator can be used to save cost and space in the generation of continuous phase modulated signals (col. 2, lines 47-63). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize an interpolator as taught by Eriksson in the place of the frequency divider of Shurboff because the interpolator could be used to generate continuous phase modulated signals with less space and cost requirements.

14. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iga in view of Eriksson.

Regarding claim 28, Iga discloses the limitations of claim 27 as applied above. Iga discloses the frequency dividing element, but does not explicitly disclose that the frequency dividing element comprises is coupled to an interpolator. However, Eriksson teaches an analogous phase lock loop apparatus wherein the frequency divider coupled to an interpolator or fractional-N modulator (fig. 1, refs. 28 and 38; col. 2, lines 47-63). Eriksson teaches that the use of an interpolator is advantageous because it can create a PLL having a higher frequency resolution and a higher bandwidth. Further, Eriksson teaches that the interpolator can be used to save cost and space in the generation of continuous phase modulated signals (col. 2, lines 47-63). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was

made to utilize an interpolator as taught by Eriksson coupled to the frequency divider of Iga because the interpolator could be used to generate continuous phase modulated signals with less space and cost requirements.

15. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iga in view of Hatchett et al (US 4378509; hereafter "Hatchett").

Regarding claim 14, Iga discloses the limitations of claim 13 as applied above. Iga discloses a stretching element coupled to the output of one of the storage elements but does not explicitly disclose a delay element coupled to the output of the logic element having an output coupled to the reset input of at least one of the first and second storage elements. However, Hatchett teaches a closely analogous phase detector apparatus by figure 1 having a delay (24) coupled to the output of a logic device (23) combining the outputs of two storage elements (20 and 21) with an output connected to the reset inputs of the storage elements. Hatchett teaches that phase detectors may suffer from a region of non-linear operation (col. 1, lines 20-48). Hatchett further teaches that the delay is provided to correct for the region of non-linearity (col. 1, lines 44-48 and lines 64-68; col. 3, lines 30-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a delay between the logic element and the reset inputs of the storage elements as taught by Hackett in the apparatus of Iga because it could be utilized to further correct for the non-linear operation of the phase detector.

Regarding claim 15, Iga in view of Hackett disclose the limitations of claim 14 as applied above. Further, in the combination of Iga in view of Hackett, because the delay

is between the logic element and the reset of the storage elements as shown by Hackett (fig. 1), the delay element is coupled to at least the reset element of the first storage element.

Regarding claim 16, Iga in view of Hackett disclose the limitations of claim 14 as applied above. Further, in the combination of Iga in view of Hackett, because the delay is between the logic element and the reset of the storage elements as shown by Hackett (fig. 1), the delay element is coupled to at least the reset element of the second storage element.

Regarding claim 17, Iga in view of Hackett disclose the limitations of claim 14 as applied above. Further, in the combination of Iga in view of Hackett, the delay is between the logic element and the reset of both of the storage elements as shown by Hackett (fig. 1).

Allowable Subject Matter

16. Claims 18, 19, and 25 are indicated to contain allowable subject matter.

17. The following is a statement of reasons for the indication of allowable subject matter:

Claims 18, 19, and 25 are indicated to contain allowable subject matter over the prior art of record because the claims are not anticipated alone or obviated in view of the collective prior art. In particular the stretching of the trailing edge output of one of the first or second storage elements in respect to the other is not disclosed or taught by the prior art as claimed in claims 18 and 19. The prior art discloses a *delay* at a one of the outputs of the storage elements with respect to another but does not disclose the

stretching of an output of one storage element with respect to another. With respect to claim 25, the prior art of record does not disclose the use of two independent stretching elements.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to phase detectors which correct for regions of non-linearity.

U.S. Pat. No. 4970475 to Gillig.

U.S. Pat. No. 6327319 to Hietala et al.

U.S. Pat. No. 6636079 to Koyama.

U.S. Pat. No. 6359945 to Doblar.

U.S. Pat. No. 6192094 to Herrmann et al.

U.S Pat. No. 6157218 to Chen.

U.S. Pat. No. 6150889 to Gulliver et al.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
December 7, 2004

jmp

CHIEH M. FAN
PRIMARY EXAMINER